

**Notice of Allowability**

Application No.

10/039,597

Applicant(s)

DAVID, HOWARD S.

Examiner

Art Unit

Zhuo H Li

2186

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 8/25/2004.
2. ☒ The allowed claim(s) is/are 1-27.
3. ☒ The drawings filed on 31 December 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some\* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

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**EXAMINER'S AMENDMENT AND STATEMENT OF REASONS FOR ALLOWANCE**

**EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the specification, Pp [0017], lines 3-4,

The interconnect 265 may include [8] 18 differential pairs, 9 pairs for data, and 9 pairs for address and command.

**EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE**

2. Claims 1-27 are allowed.
3. The following is an examiner's statement of reasons for allowance:

Applicant's invention is draw to a method and apparatus for performing the tag look-ups in parallel with the memory module decodes in the memory controller in order to improves latency for cache hits without penalizing the latency for cache misses (i.e., memory controller comprising a plurality of tag units to perform tag look-up operations in response to a memory access request, and memory module decode unit perform decode operations to determine which one of the plurality of modules in being access by the

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memory access request substantially concurrently with respect to the tag look-up operations wherein a data cache located each of the memory modules).

Applicant's independent claims 1 and 10 each recites, *inter alia*, a memory controller (202) with a structure defined in the specification (pages 4-12) comprising a plurality of tag units (400, 340, 350 and 360), each tag unit including any array of tag address storage locations, the plurality of tag units to perform tag look-up operations in response a memory access request, a memory module decode unit (320) to perform decode operations to determine which one of a plurality of memory modules is being accessed by the memory access request substantially concurrently with respect to the tag look-up operations, and a command sequencer and serializer unit (380) couple to the array of tag address storage location and the memory module decode unit (figure 3), the command sequencer and serializer unit to serialize commands and address information and sequentially transmit over a serial link of a memory bus coupling the memory control with a plurality of memory modules (220-250), to a memory module to access a data cache (222, 232, 242, 252) located on the memory module (220-250), respectively, that is specified by the memory module decode unit as a result of the decode operations, if the lookup operations indicate that at least one of the tag addresses matches a memory address of the memory access request. Applicant's invention of claim 1 and 10 each comprises a particular combination of elements, which is neither taught nor suggested by the prior art.

Applicant's independent method claim 16 recites, *inter alia*, the steps of performing a tag look-up by a plurality of tag units within the memory controller to determine whether there is a cache hit for the read request, each tag unit including an

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array of tag address storage locations, determining by a memory module decode unit which of a plurality of memory modules is addressed by the read request, wherein performing a tag look-up and determining which of a plurality of memory modules is addressed by the read request occur in parallel, and fetching by a command sequencer and serializer unit coupled to the tag units and the memory module decode unit a line of cache data from a data cache located on one of the plurality of memory modules if the tag look-up indicates a cache hit, the memory modules separate from the memory controller and coupled to the memory controller via a memory bus. These steps, in combination with the remaining steps of claims 17 and 18, are neither taught nor suggested by the prior art.

Accordingly, Applicant's claims are allowed for these reasons and for the reasons recited by Applicant's amendments filed on (12/31/2003 and 08/30/2004).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."


4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183.

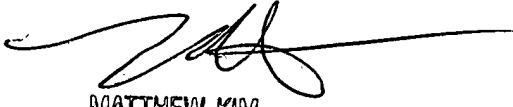
The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li   
Patent Examiner  
Art Unit 2186

  
MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY AND SYSTEMS  
MATTHEW KIM  
TC 2100

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